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PATENT & TRADEMARK OFFICE

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of: Attorney Docket No.: 2470.02US02

Meyer

Application No.: 09/899,763 Examiner: Not Assigned

Filed: July 5, 2001 Group Art Unit: 2123

For: DIGITAL AND ANALOG MIXED SIGNAL SIMULATION USING PLI API

LETTER TO THE OFFICIAL DRAFTSPERSON

Assistant Commissioner for Patents
Attention: Official Draftsperson
Washington, D.C. 20231

Sir:

Informal drawings were submitted for filing with the above-identified patent application. Enclosed for filing are thirteen (13) sheets (Figs. 1-10) of formal drawings.

Respectfully submitted,

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Please grant any extension of time necessary for entry; charge any fee due to Deposit Account No. 16-0631.

CERTIFICATE OF MAILING

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October 16, 2001
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Kimberly K. Baxter

Fig. 1

```
1  // DIVIDER FROM VERILOG-AMS STANDARIZATION
       COMMITTEE PUBLIC CIRCUITS
2  'TIMESCALE 10NS/1NS
3  'INCLUDE "DECIPLINES.H"
4  'INCLUDE "CONNECT.H"
5
6  MODULE TOP;
7  REG CLK;
8  WIRE SYS_CLK;
9
10 // DIGITAL CONSTRUCTS
11 INITIAL CLK=0;
12 ALWAYS #5 CLK = ~CLK;
13 ASSIGN SYS_CLK = CLK;
14
15 // INSTANTIATIONS
16 ZDETECT MY_DEV(SYS  CLK, DIVOUT);
17 LPF #(.TAU(1.59E-8)) TENMLPF(DIVOUT, TENOUT);
18 ENDMODULE
19
20 MODULE ZDETECT (IN, OUT);
21 INPUT IN;
22 OUTPUT OUT;
23 ELECTRICAL IN,OUT;
24 INTEGER N, STATE;
25 PARAMETER DIV = 5;
26
27 // ANALOG BLOCKS CODE ANALOG CIRCUITS AS EQUATIONS
28 ANALOG BEGIN
29 @(CROSS(V(IN) - 2.5, +1)) N = N + 1;
30 IF (N >=DIV) BEGIN
31  IF (STATE ==≠ 0) STATE = 1
32 ELSE STATE ≠ 0;
33 N = 0;
34 END
35 V(OUT) <+STATE * 5;
36 END ENDMODULE
37
38 MODULE LPF(IN, OUT);
39 INOUT IN, OUT;
40 ELECTRICAL IN, OUT;
41 PARAMETER REAL TAU = 1E-3;
42
43 ANALOG
44 BEGIN
45 V(OUT)<+LAPLACE_ND(V(IN), {1.0}, {1.0 TAU});
46 END
47 ENDMODULE
```

Fig. 2

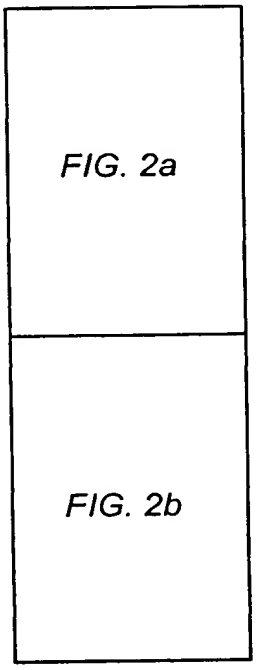


Fig. 8

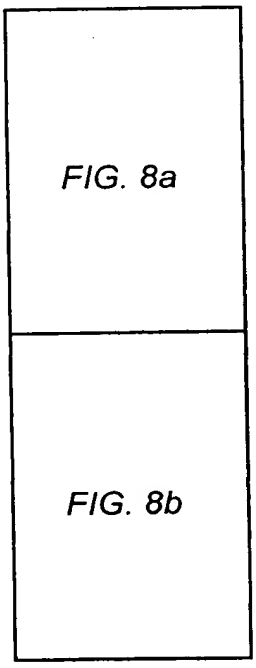


Fig. 2a

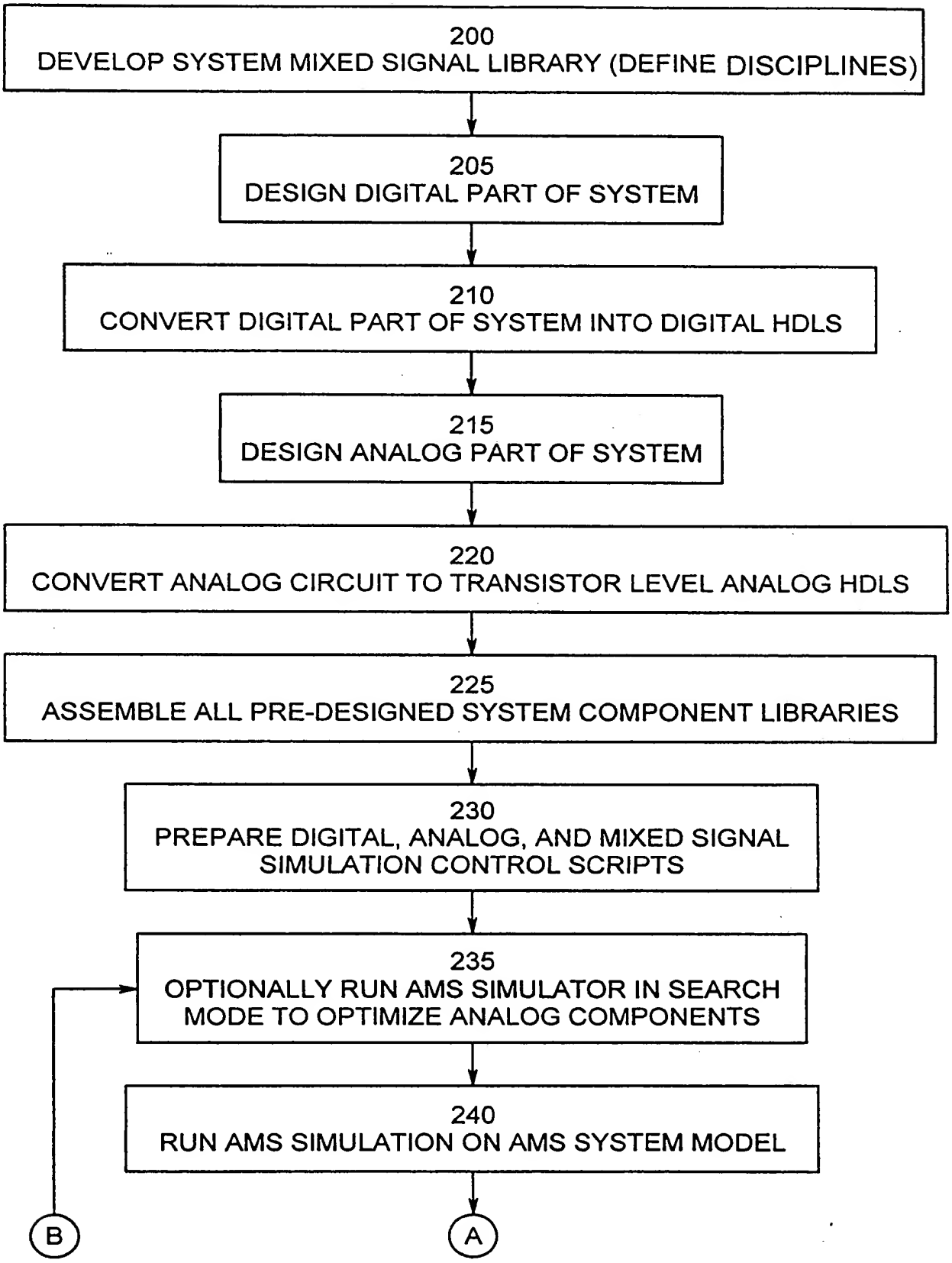

200
DEVELOP SYSTEM MIXED SIGNAL LIBRARY (DEFINE DISCIPLINES)
205
DESIGN DIGITAL PART OF SYSTEM
210
CONVERT DIGITAL PART OF SYSTEM INTO DIGITAL HDLS
215
DESIGN ANALOG PART OF SYSTEM
220
CONVERT ANALOG CIRCUIT TO TRANSISTOR LEVEL ANALOG HDLS
225
ASSEMBLE ALL PRE-DESIGNED SYSTEM COMPONENT LIBRARIES
230
PREPARE DIGITAL, ANALOG, AND MIXED SIGNAL SIMULATION CONTROL SCRIPTS
235
OPTIONALLY RUN AMS SIMULATOR IN SEARCH MODE TO OPTIMIZE ANALOG COMPONENTS
240
RUN AMS SIMULATION ON AMS SYSTEM MODEL
B
A

Fig. 2b

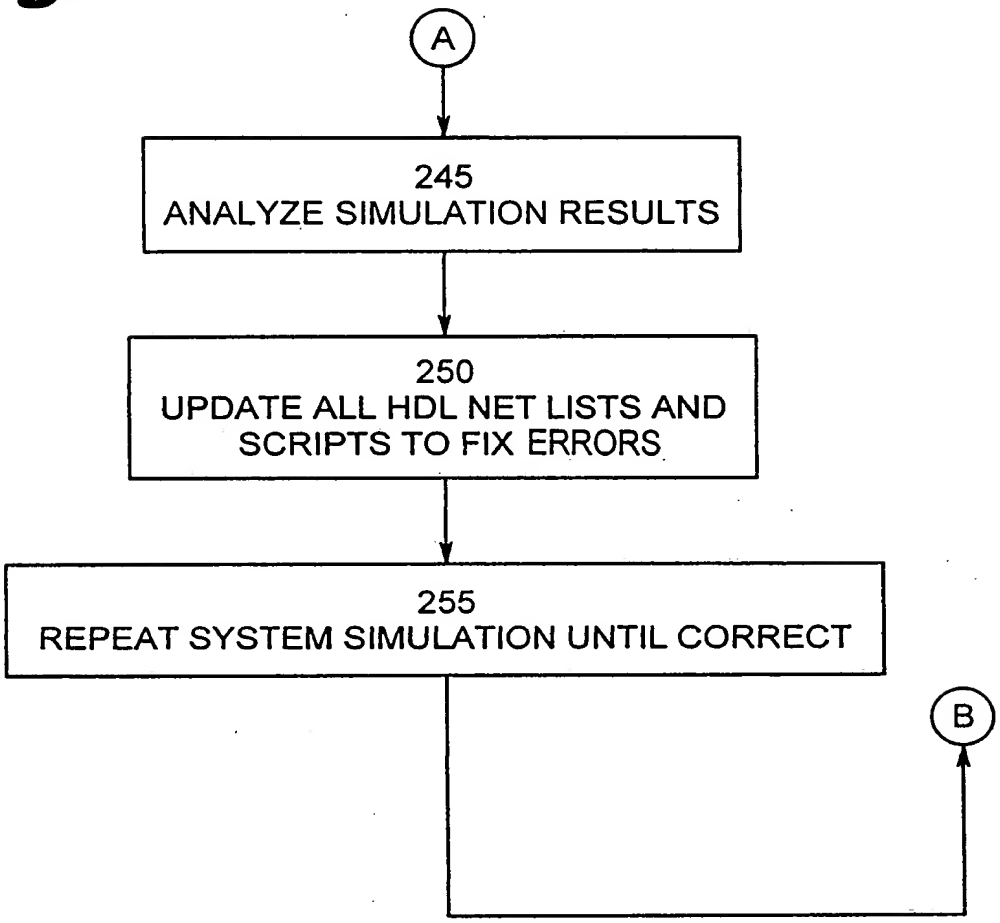

A
245
ANALYZE SIMULATION RESULTS
250
UPDATE ALL HDL NET LISTS AND SCRIPTS TO FIX ERRORS
255
REPEAT SYSTEM SIMULATION UNTIL CORRECT
B

Fig. 3

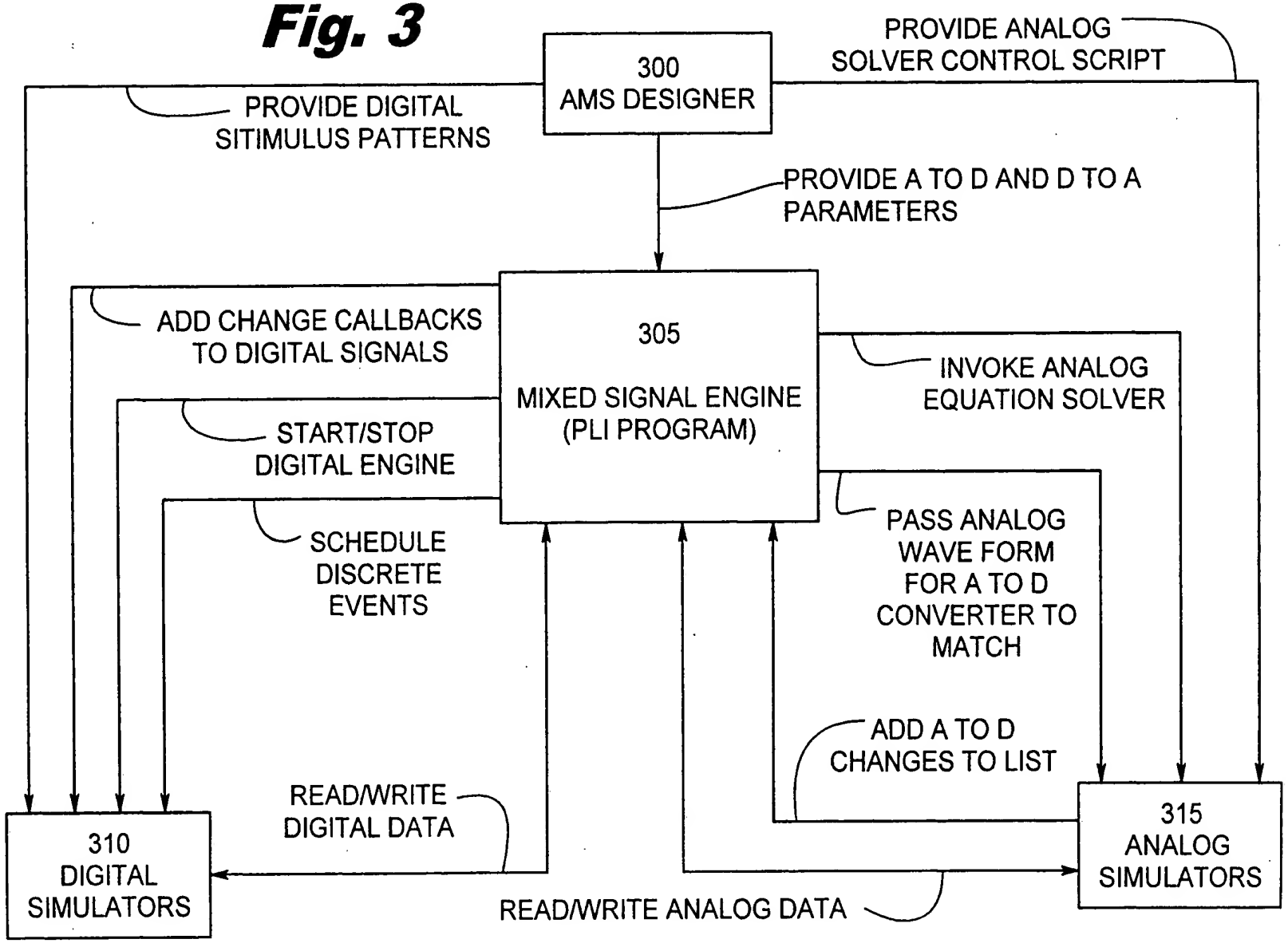

300
AMS DESIGNER
PROVIDE ANALOG
SOLVER CONTROL SCRIPT
PROVIDE DIGITAL
SITIMULUS PATTERNS
PROVIDE A TO D AND D TO A
PARAMETERS
305
MIXED SIGNAL ENGINE
(PLI PROGRAM)
ADD CHANGE CALLBACKS
TO DIGITAL SIGNALS
INVOKE ANALOG
EQUATION SOLVER
START/STOP
DIGITAL ENGINE
SCHEDULE
DISCRETE
EVENTS
PASS ANALOG
WAVE FORM
FOR A TO D
CONVERTER TO
MATCH
ADD A TO D
CHANGES TO LIST
READ/WRITE
DIGITAL DATA
310
DIGITAL
SIMULATORS
315
ANALOG
SIMULATORS
READ/WRITE ANALOG DATA

Fig. 4

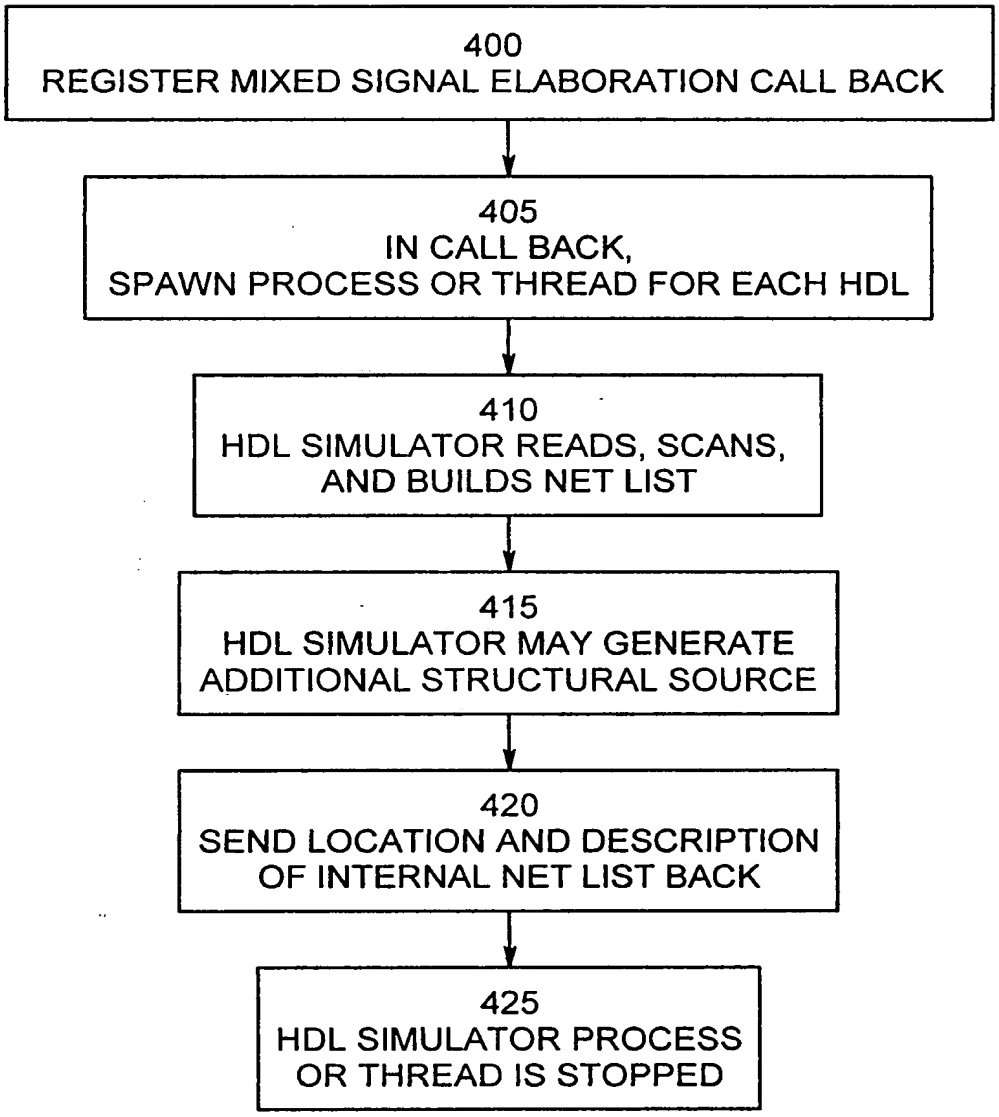

400
REGISTER MIXED SIGNAL ELABORATION CALL BACK
405
IN CALL BACK,
SPAWN PROCESS OR THREAD FOR EACH HDL
410
HDL SIMULATOR READS, SCANS,
AND BUILDS NET LIST
415
HDL SIMULATOR MAY GENERATE
ADDITIONAL STRUCTURAL SOURCE
420
SEND LOCATION AND DESCRIPTION
OF INTERNAL NET LIST BACK
425
HDL SIMULATOR PROCESS
OR THREAD IS STOPPED

Fig. 5

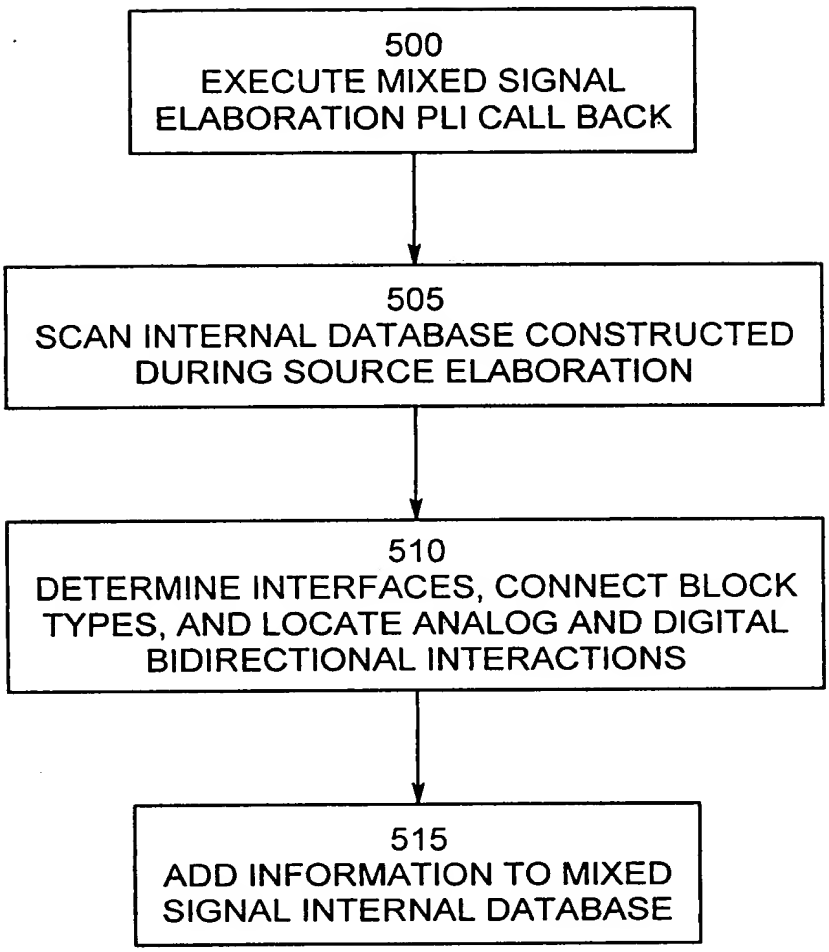

500
EXECUTE MIXED SIGNAL ELABORATION PLI CALL BACK
505
SCAN INTERNAL DATABASE CONSTRUCTED DURING SOURCE ELABORATION
510
DETERMINE INTERFACES, CONNECT BLOCK TYPES, AND LOCATE ANALOG AND DIGITAL BIDIRECTIONAL INTERACTIONS
515
ADD INFORMATION TO MIXED SIGNAL INTERNAL DATABASE

Fig. 6

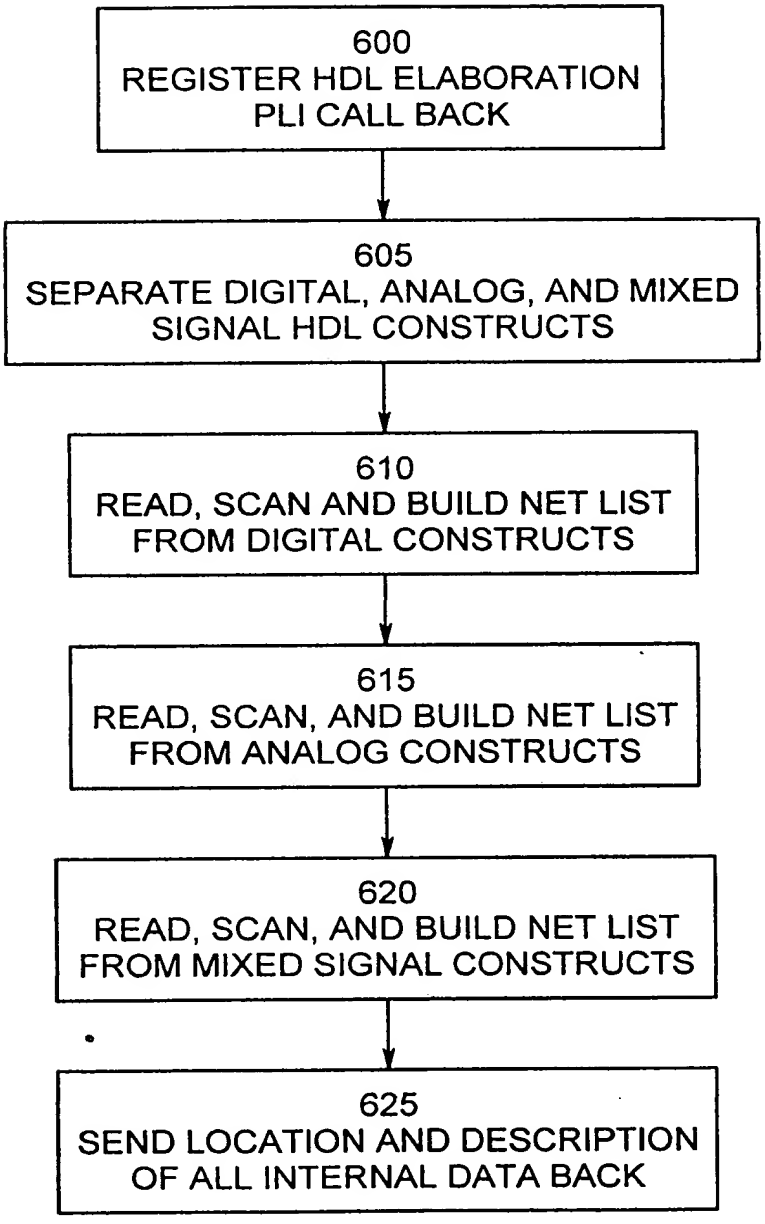

600
REGISTER HDL ELABORATION PLI CALL BACK
605
SEPARATE DIGITAL, ANALOG, AND MIXED SIGNAL HDL CONSTRUCTS
610
READ, SCAN AND BUILD NET LIST FROM DIGITAL CONSTRUCTS
615
READ, SCAN, AND BUILD NET LIST FROM ANALOG CONSTRUCTS
620
READ, SCAN, AND BUILD NET LIST FROM MIXED SIGNAL CONSTRUCTS
625
SEND LOCATION AND DESCRIPTION OF ALL INTERNAL DATA BACK

Fig. 7

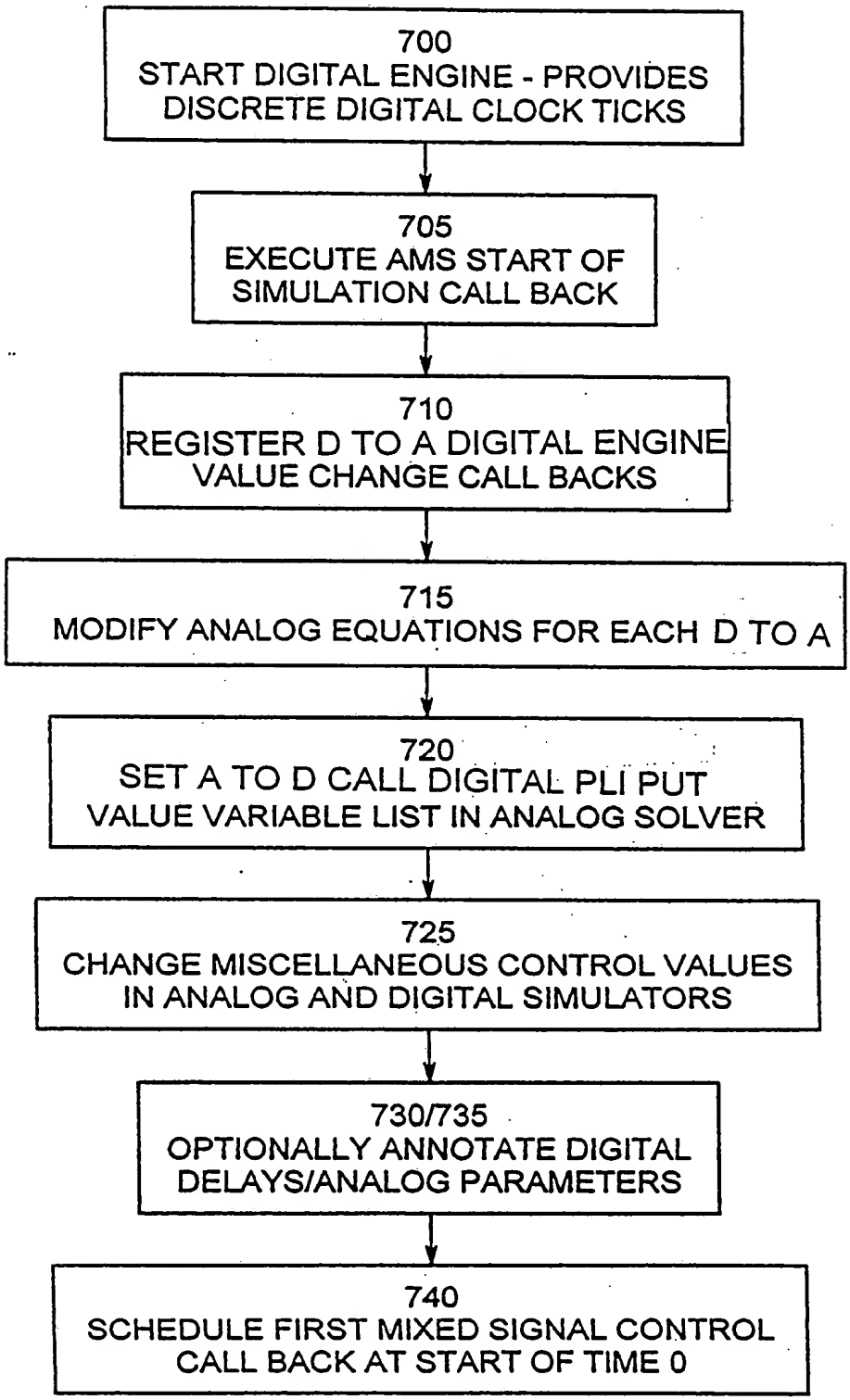

700
START DIGITAL ENGINE - PROVIDES DISCRETE DIGITAL CLOCK TICKS
705
EXECUTE AMS START OF SIMULATION CALL BACK
710
REGISTER D TO A DIGITAL ENGINE VALUE CHANGE CALL BACKS
715
MODIFY ANALOG EQUATIONS FOR EACH D TO A
720
SET A TO D CALL DIGITAL PLI PUT VALUE VARIABLE LIST IN ANALOG SOLVER
725
CHANGE MISCELLANEOUS CONTROL VALUES IN ANALOG AND DIGITAL SIMULATORS
730/735
OPTIONALLY ANNOTATE DIGITAL DELAYS/ANALOG PARAMETERS
740
SCHEDULE FIRST MIXED SIGNAL CONTROL CALL BACK AT START OF TIME 0

Fig. 8a

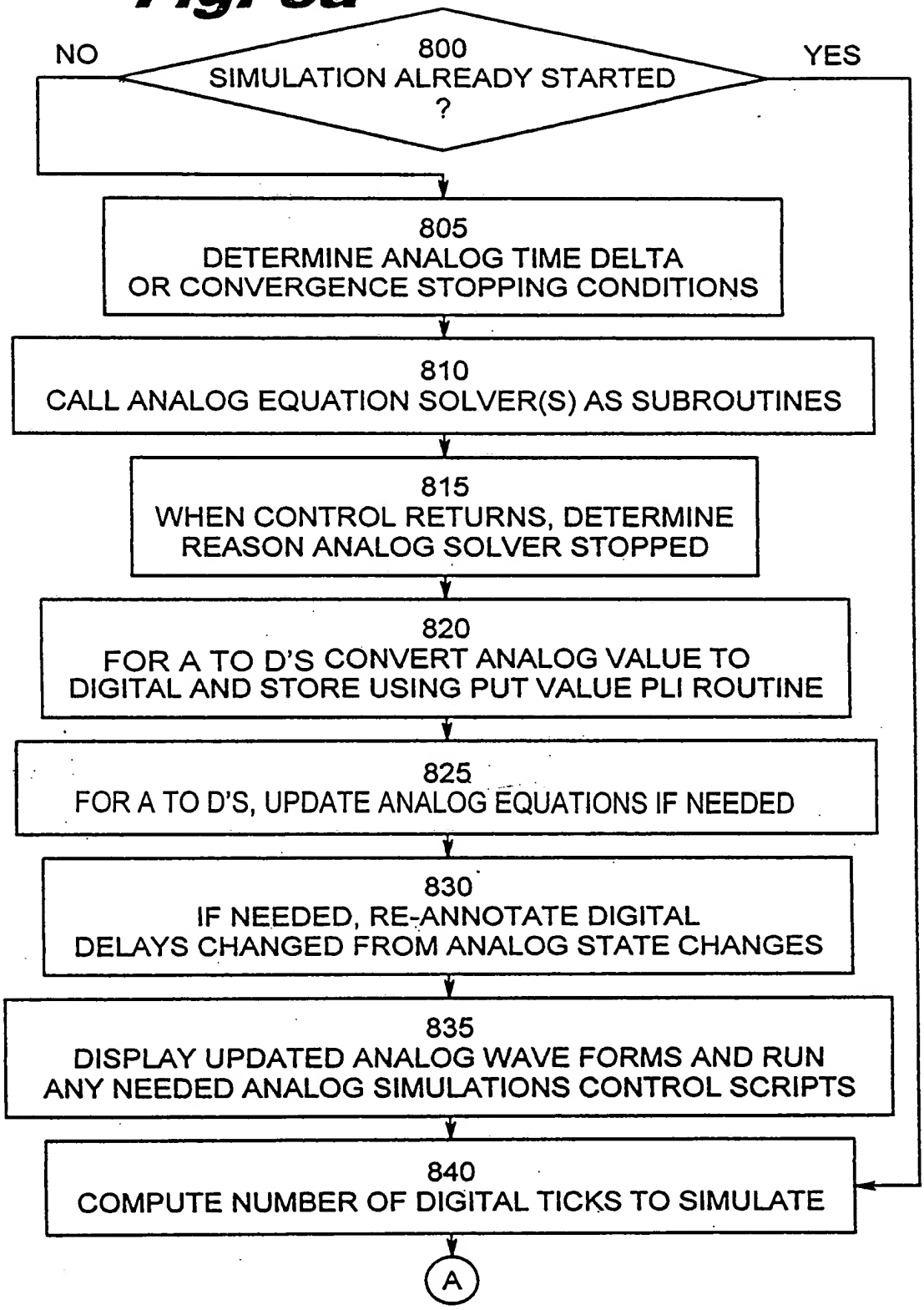

800
SIMULATION ALREADY STARTED
?
NO
YES
805
DETERMINE ANALOG TIME DELTA
OR CONVERGENCE STOPPING CONDITIONS
810
CALL ANALOG EQUATION SOLVER(S) AS SUBROUTINES
815
WHEN CONTROL RETURNS, DETERMINE
REASON ANALOG SOLVER STOPPED
820
FOR A TO D'S CONVERT ANALOG VALUE TO
DIGITAL AND STORE USING PUT VALUE PLI ROUTINE
825
FOR A TO D'S, UPDATE ANALOG EQUATIONS IF NEEDED
830
IF NEEDED, RE-ANNOTATE DIGITAL
DELAYS CHANGED FROM ANALOG STATE CHANGES
835
DISPLAY UPDATED ANALOG WAVE FORMS AND RUN
ANY NEEDED ANALOG SIMULATIONS CONTROL SCRIPTS
840
COMPUTE NUMBER OF DIGITAL TICKS TO SIMULATE
A

Fig. 8b

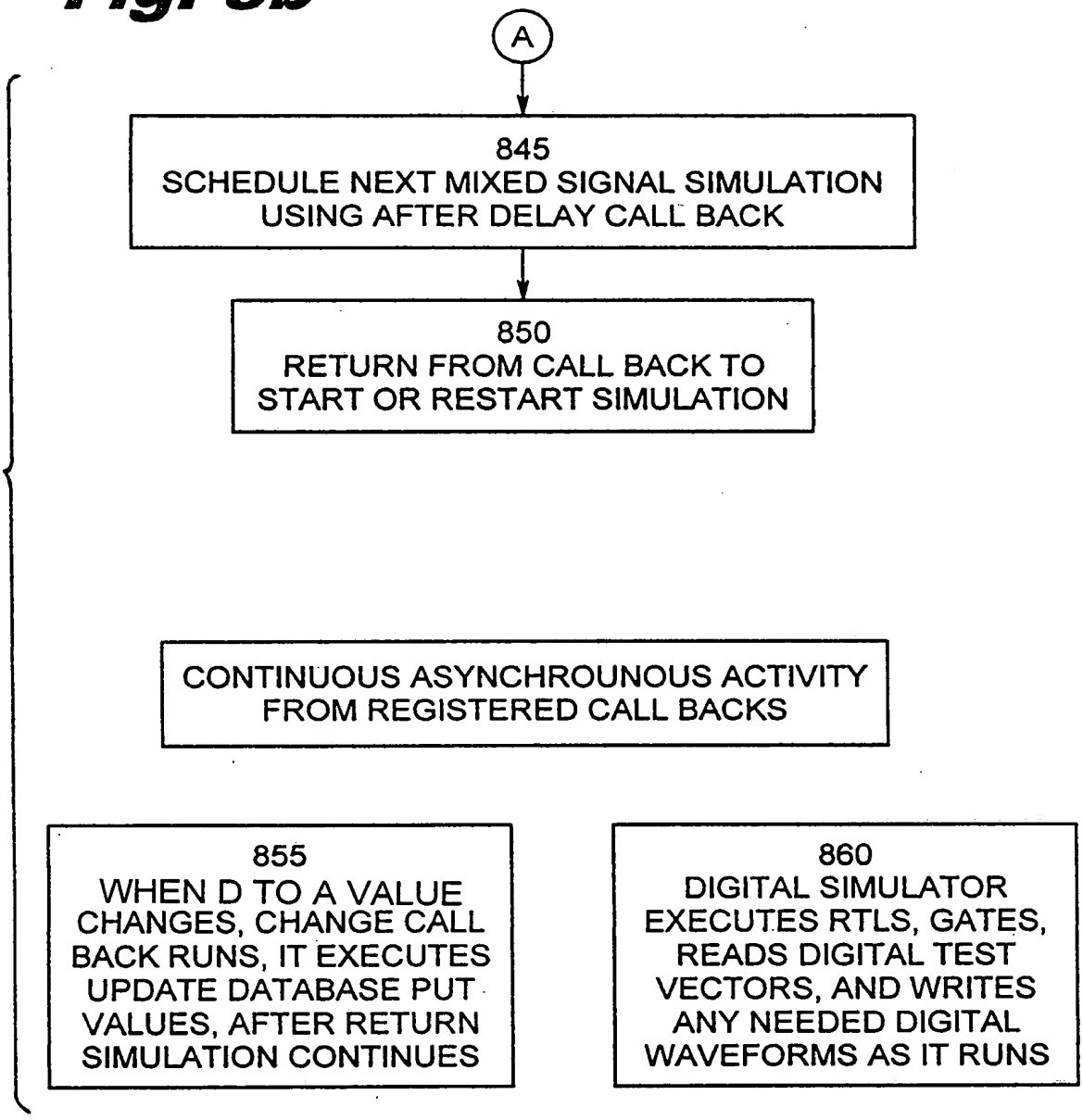

A
845
SCHEDULE NEXT MIXED SIGNAL SIMULATION USING AFTER DELAY CALL BACK
850
RETURN FROM CALL BACK TO START OR RESTART SIMULATION
CONTINUOUS ASYNCHROUNOUS ACTIVITY FROM REGISTERED CALL BACKS
855
WHEN D TO A VALUE CHANGES, CHANGE CALL BACK RUNS, IT EXECUTES UPDATE DATABASE PUT VALUES, AFTER RETURN SIMULATION CONTINUES
860
DIGITAL SIMULATOR EXECUTES RTLS, GATES, READS DIGITAL TEST VECTORS, AND WRITES ANY NEEDED DIGITAL WAVEFORMS AS IT RUNS

Fig. 9

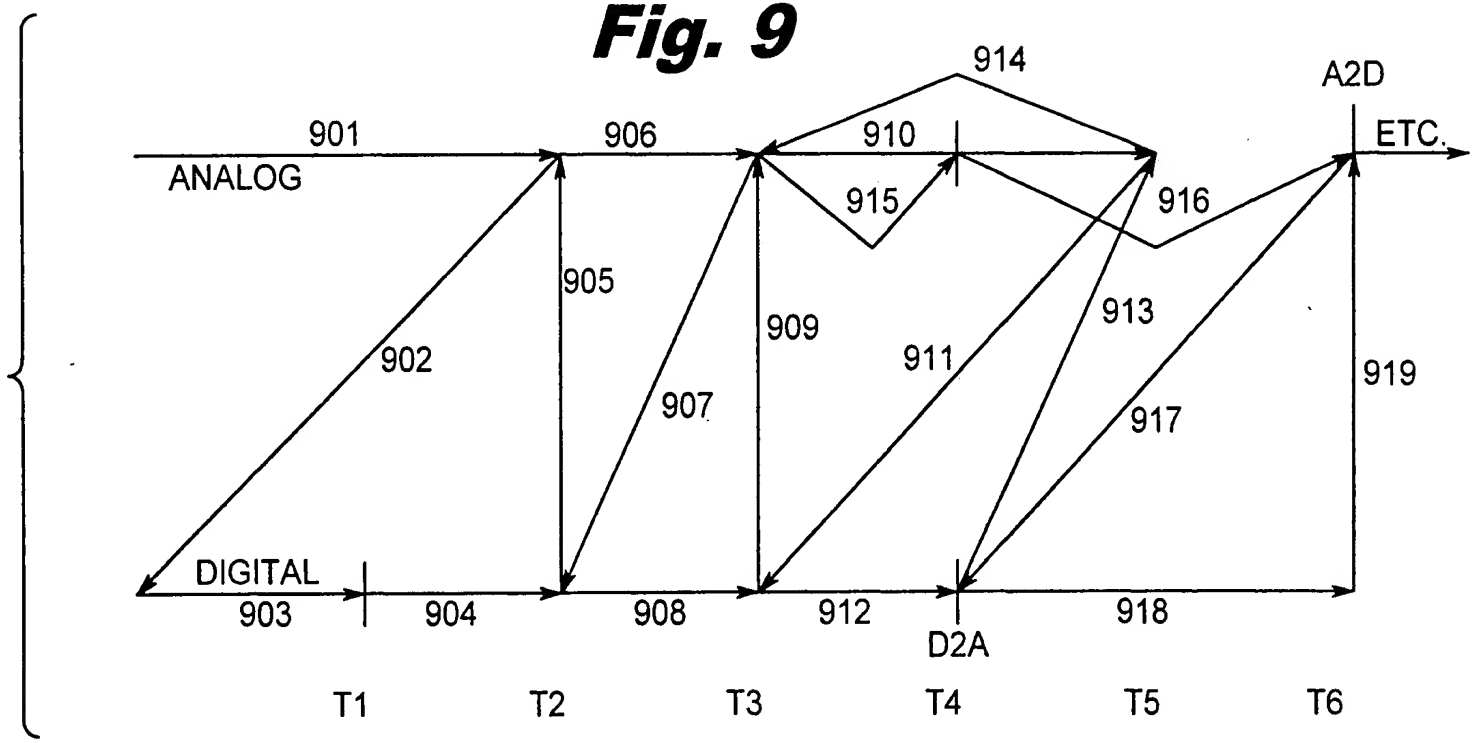
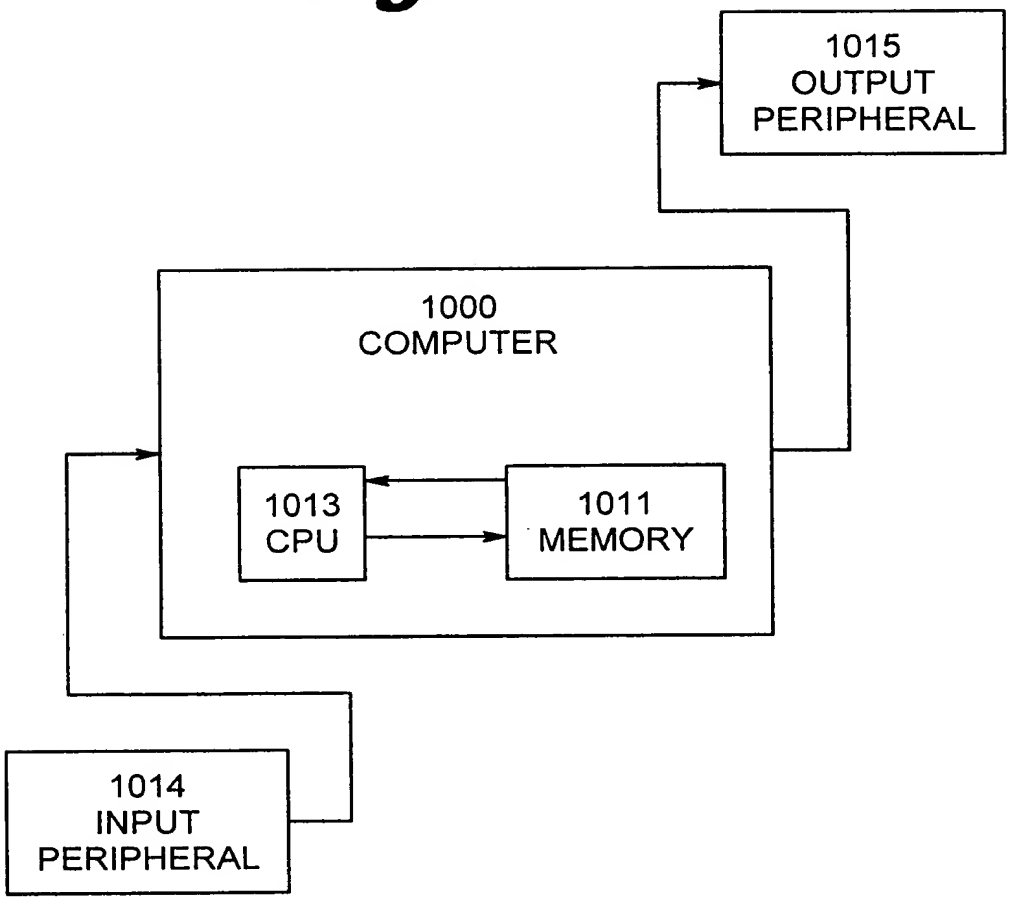

914
A2D
901
906
910
ETC.
ANALOG
915
916
905
913
902
909
911
919
907
917
DIGITAL
903
904
908
912
D2A
918
T1
T2
T3
T4
T5
T6

Fig. 10


1015
OUTPUT
PERIPHERAL
1000
COMPUTER
1013
CPU
1011
MEMORY
1014
INPUT
PERIPHERAL